AMENDMENTS TO THE CLAIMS

1-6 (Canceled).

7. (Original) A liquid crystal display comprising:

a substrate;

a gate wire on the substrate, the gate wire including a gate electrode and gate line;

a gate insulating layer covering an exposed surface of the substrate including the gate wire;

a thin film transistor formed in an active layer on the gate insulating layer, the thin film transistor having the gate electrode and further having a source electrode and a drain electrode;

a data wire on the gate insulating layer, the data wire including a data line, the source electrode, and the drain electrode;

a pixel electrode connected to the drain electrode of the thin film transistor; and

a passivation layer covering the data wire and the thin film transistor, except the drain electrode, the passivation layer being covered by the pixel electrode, the passivation layer exposing the gate insulating layer except portions of the gate insulating layer where the data wire, the thin film transistor, and pixel electrode are formed;

a data pad at an end of the data line, said data pad being covered with the passivation layer;

a contact hole in the passivation layer, the contact hole exposing an exposed portion of the data pad; and

a data pad covering layer covering the exposed portion of the data pad.

8. (Canceled).

9. (Previously Presented) The liquid crystal display according to claim 7, wherein a part of the data wire on the gate insulating layer over the gate line comprises a subsidiary electrode, and

wherein the subsidiary electrode comprises an exposed portion and a remainder portion being covered with the passivation layer, and wherein the exposed portion of the subsidiary electrode is connected to a pixel electrode.

10. (Original) The liquid crystal display according to claim 7, wherein the passivation layer covers the data wire and thin film transistor, and exposes a portion of the pixel electrode.

11. (Currently Amended) The liquid crystal display according to claim 7, ~~wherein the~~ further including a photoresist pattern ~~covers~~ covering the data wire and the thin film transistor ~~the data pad~~.

12. (New) A liquid crystal display comprising:

a substrate;

a gate wire on the substrate, the gate wire including a gate electrode and gate line;

a gate insulating layer covering an exposed surface of the substrate including the gate wire;

a thin film transistor formed in an active layer on the gate insulating layer, the thin film transistor having the gate electrode and further having a source electrode and a drain electrode;

a data wire on the gate insulating layer, the data wire including a data line, the source electrode, and the drain electrode;

a passivation layer covering the data wire and the thin film transistor, the passviation having a contact hole on the drain electrode;

a pattern defect on the gate insulating layer;

a pixel electrode on the passivation layer, the pixel electrode being connected to the drain electrode through the contact hole,

wherein the pattern defect is opened by removing partially the passivation layer.

13. (New) The liquid crystal display according to claim 12, wherein the gate insulating layer except portions of the gate insulating layer where the data wire, the thin film transistor, and pixel electrode are formed are exposed.

14. (New) The liquid crystal display according to claim 12, wherein the pattern defect is generated from residue of a substance used to form a active layer of the thin film transistor.

15. (New) The liquid crystal display according to claim 12, wherein the pattern defect is generated from residue of a substance used to form the data wire.

16. (New) A liquid crystal display comprising:

a substrate;

a gate wire on the substrate, the gate wire including a gate electrode and gate line;

a gate insulating layer covering an exposed surface of the substrate including the gate wire;

a thin film transistor formed in an active layer on the gate insulating layer, the thin film transistor having the gate electrode and further having a source electrode and a drain electrode;

a data wire on the gate insulating layer, the data wire including a data line, the source electrode, and the drain electrode;

a pixel electrode connected to the drain electrode of the thin film transistor;

a passivation layer covering the data wire and the thin film transistor, except the drain electrode, the passivation layer being covered by the pixel electrode, the passivation layer at the portion where a pattern defect is disposed being removed to expose the gate insulating layer except portions of the gate insulating layer where the data wire, the thin film transistor, and pixel electrode are formed;

a data pad at an end of the data line, said data pad being covered with the passivation layer;

a contact hole in the passivation layer, the contact hole exposing an exposed portion of the data line; and

a data pad covering layer covering the exposed portion of the data pad.